W2112

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/JP02/09437

I. Basis of the report

1. With regard to the **elements** of the international application:*

- [ ] the international application as originally filed.
- [X] the description:
  - pages 1-23, as originally filed,
  - pages _____, filed with the demand,
  - pages _____, filed with the letter of _____
- [X] the claims:
  - claims 1-2, 4-6, 9-12, as originally filed,
  - claims _____, as amended (together with any statement under Article 19)
  - claims _____, filed with the demand,
  - claims 3, 7, 8, filed with the letter of 14. 03. 03
- [X] the drawingss:
  - pages 1-15, as originally filed,
  - pages _____, filed with the demand,
  - pages _____, filed with the letter of _____
- [ ] the sequence listing part of the description:
  - pages _____, as originally filed,
  - pages _____, filed with the demand,
  - pages _____, filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless oterwise indicated under this item.

These elements were available or furnished to this Authority in the following language _____ which is:

- [ ] the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).
- [ ] the language of publication of the intenational application (under Rule 48.3(b)).
- [ ] the language of the translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3)

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- [ ] contained in the international application in written form.
- [ ] filed together with the international application in computer readable form.
- [ ] furnished subsequently to this Authority in written form.
- [ ] furnished subsequently to this Authority in computer readable form.
- [ ] The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- [ ] The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. [ ] The amendments have resulted in the cancellation of:
   - [ ] the description, pages _____
   - [ ] the claims, Nos. _____
   - [ ] the drawings, sheets/fig. _____

5. [ ] This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rule 70.16 and 70.17).*

** *Any replacement sheet containing such amendments must be referred to under item I and annexed to this report.*

CLAIMS

1. A semiconductor device for executing software including an arithmetic instruction, comprising:

a register;

an ALU;

an arithmetic circuit including a plurality of arithmetic cells and a plurality of register cells for setting a calculation type to be executed by said arithmetic cells and wiring connections between said plurality of arithmetic cells and said plurality of register cells; and

a control circuit for generating set data for setting said calculation type of the arithmetic cells and said wiring connections and also generating driver software for performing operation equivalent to said software using said arithmetic circuit on the basis of said software.

2. A semiconductor device according to claim 1, wherein said control circuit is arranged to generate said set data and said driver software during execution of said software using said register and said ALU.

3. A semiconductor device according to claim 2, wherein processing of said software is repeated n times, the processing of said software from the first time to the i-th (i<n) time is carried out by executing said software using said register and said ALU, and the processing of the software from the (i+1)-th time to the n-th time is carried out by executing said driver

software using said arithmetic circuit.

4. A semiconductor device according to claim 1, wherein said driver software includes at least a data transfer instruction from said register to the register cell of said arithmetic circuit and a data transfer instruction from the register cell of said arithmetic circuit to said register.

5. A semiconductor device according to claim 1, wherein said control circuit generates said set data and said driver software by executing the software for generating said set data and said driver software.

6. A semiconductor device according to claim 1, wherein said arithmetic circuit is connected to a bus.

7. A semiconductor device according to claim 1, wherein the number of clock cycles necessary for executing said software is smaller than the number of clock cycles necessary for executing said driver software.

8. A semiconductor device for executing software including an arithmetic instruction, comprising:

a register;

an ALU;

an arithmetic circuit includi8ng a plurality of arithmetic cells and a plurality of register cells for setting an calculation type to be executed by said arithmetic cells and wiring connections between said plurality of arithmetic cells and said plurality of register cells;

a first memory area for storing said software;

a second memory area for storing driver software for performing operation equivalent to said software; and

a control circuit for controlling the software to be executed,

wherein processing of said software is repeated n times, the processing thereof from the first time to the i-th time (i<n) is carried out by executing said software read out from said first memory area using said register and said ALU, said control circuit in response to said first time processing switches the software to be executed to said driver software, and the processing from the (i+1)-th time to the n-th time is carried out by executing said driver software read out from said second memory area using said arithmetic circuit.

9. A semiconductor device according to claim 8, wherein said control circuit generates set data for setting the calculation type of said arithmetic cell and said wiring connections on the basis of said software and driver software for performing operation equivalent to said software.

10. A semiconductor device according to claim 8, wherein said control circuit has set data for setting the calculation type of the arithmetic circuit and said wiring connections, and said arithmetic circuit sets

the calculation type of said arithmetic cells and said wiring connections.

11. A semiconductor device according to claim 8, wherein said driver software includes at least a data transfer instruction from said register to the register cell of said arithmetic circuit and a data transfer instruction from the register cell of said arithmetic circuit to said register.

12. A semiconductor device according to claim 8, wherein the number of clock cycles necessary for executing said driver software is smaller than the number of clock cycles necessary for executing said software.